

## SSC8L61GS1

#### **P-Channel Enhancement Mode MOSFET**

#### Features

V <sub>DS</sub>	$V_{GS}$	R <sub>DS(ON)</sub> Typ.	Ι <sub>D</sub>	
-60V	$\pm 20 V$	18mΩ@-10V	-30A	

## Description

This device is P-Channel enhancement MOSFET.

Uses SGT technology and design to provide excellent

RDSON with low gate charge. This device is suitable
for use in DC-DC conversion, power switch and
charging circuit.

#### 100% UIS + ΔVDS + Rg Tested!

#### Applications

- Load Switch
- PWM Application
- Power Management

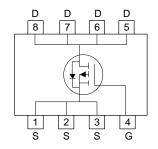
#### Ordering Information

Device	Package	Shipping		
SSC8L61GS1	SOP-8	4000/Reel		

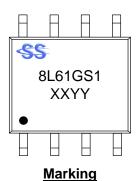
### Pin configuration



SOP-8



Pin Configuration (Top View)



(XXYY: Internal Traceability Code)



### Absolute Maximum Ratings (T<sub>A</sub>=25<sup>°</sup>C unless otherwise noted)

Symbol	Parameter		Ratings	Unit	
$V_{DSS}$	Drain-to-Source Voltage		-60	V	
$V_{GSS}$	Gate-to-Source Voltage		±20	V	
L	Continuous Drain Current d	T <sub>C</sub> =25°C	-30	^	
l <sub>D</sub>		T <sub>C</sub> =100°C	-15	Α	
	Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =25°C	-9	^	
IDSM		T <sub>A</sub> =70°C	-7	А	
I <sub>DM</sub>	Pulsed Drain Current b		-90	Α	
Б	Power Dissipation <sup>c</sup>	Tc=25°C	27.8	W	
P <sub>D</sub>		T <sub>C</sub> =100°C	11.1		
Б	Power Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	2.98	10/	
P <sub>DSM</sub>		T <sub>A</sub> =70°C	1.9	W	
Eas	Avalanche Energy b L=0.5mH Single Pulse		50	mJ	
TJ	Operation junction temperature		-55~150	°C	
T <sub>STG</sub>	Storage temperature range		-55~150		

#### ➤ Thermal Resistance Ratings (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
RθJA	Junction-to-Ambient Thermal Resistance a	42	°C/W	
$R_{ heta JC}$	Junction-to-Case Thermal Resistance	4.5	C/VV	

#### Note:

- a. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with  $T_A$ =25 °C. The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.

SSC-V1.2 www.sscsemi.com Analog Future



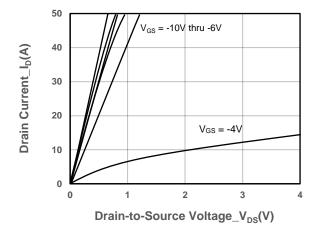


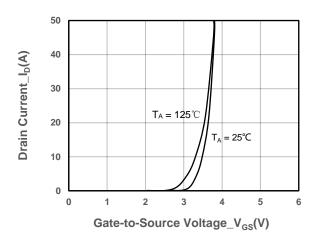
# > Electrical Characteristics (T<sub>A</sub>=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250uA$	-1	-1.8	-2.5	V
Drain-Source On-Resistance	R <sub>DS(on)</sub>	$V_{GS} = -10V, I_D = -6A$		18	28	mΩ
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = -60V, V <sub>GS</sub> = 0V			1	μA
Gate-Source Leak Current	Igss	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA
Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A		-0.75	-1.4	٧
Gate Resistance	R <sub>G</sub>	V <sub>DS</sub> = 0V, f = 1MHz		8		Ω
Input Capacitance	Ciss	V 20V/V 0V		1500		pF
Output Capacitance	Coss	$V_{DS} = -30V$ , $V_{GS} = 0V$ , $f = 1MHz$		250		
Reverse Transfer Capacitance	Crss	T = TIVIMZ		12		
Total Gate Charge	$Q_{\mathrm{G}}$	101/11/ 001/		21		nC
Gate to Source Charge	Q <sub>GS</sub>	$V_{GS} = -10V$ , $V_{DS} = -30V$ ,		3.6		
Gate to Drain Charge	$Q_{GD}$	I <sub>D</sub> = -5A		3		
Turn-on Delay Time	T <sub>D(ON)</sub>	$V_{GS} = -10V, V_{DD} = -30V,$ $R_{L} = 3\Omega, R_{G} = 3\Omega,$		16		
Rise Time	Tr			18		
Turn-off Delay Time	$T_{D(OFF)}$			40		ns
Fall Time	Tf	I <sub>D</sub> = -5A		45		



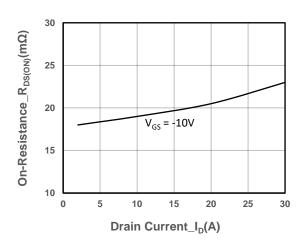
## ➤ Typical Performance Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

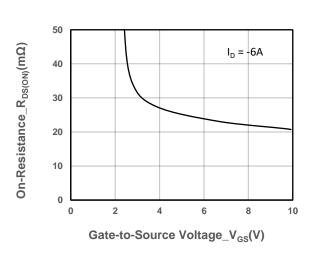




#### **Output Characteristics**

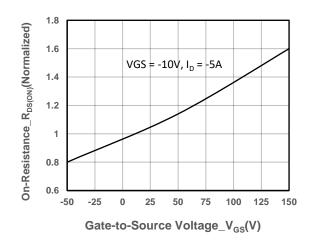


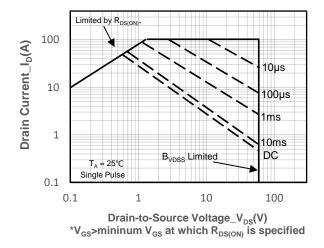




#### On-Resistance vs. Drain Current and Gate Voltag

On-Resistance vs. Gate-to-Source Voltage



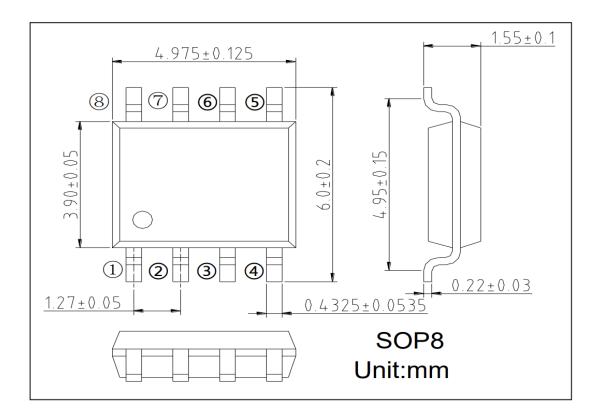


**On-Resistance vs. Junction Temperature** 

Safe Operating Area vs. Junction-to-Ambient



### Package Information



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