

SSC8043GS1

P-Channel Enhancement Mode MOSFET

Features

V _{DS}	V_{GS}	R _{DS(ON)} Typ.	l _D
-40V	±20V	22mΩ@-10V	-18A
		30mΩ@-4V5	-10/

> Description

This SSC8043GS1 uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

100% UIS + ΔVDS + Rg Tested!

Applications

- Load Switch
- PWM Application
- Power Management

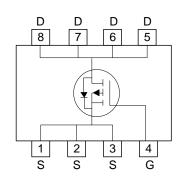
Ordering Information

Device	Package	Shipping	
SSC8043GS1	SOP-8	4000/Reel	

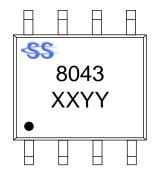
Pin configuration



SOP-8 (Top View)



Pin Configuration



Marking

(XXYY: Internal Traceability Code)



➤ Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit		
V _{DSS}	Drain-to-Source Voltage		-40	V	
V _{GSS}	Gate-to-Source Volta	Gate-to-Source Voltage		V	
	Continuous Drain Current d	T _C =25℃	-18	А	
l _D		T _C =100°C	-10		
	Continuous Drain Current ^a	T _A =25℃	-9	Δ.	
IDSM		T _A =70°C	-7	- A	
Ірм	Pulsed Drain Current ^b		-70	Α	
Б	Power Dissipation °	Tc=25℃	12.5	W	
P _D		T _C =100°C	5		
Б	Power Dissipation ^a	T _A =25℃	3.47	10/	
P _{DSM}		T _A =70°C	2.22	W	
I _{AS}	Avalanche Current b L=0.5mH Single Pulse		-10	Α	
Eas	Avalanche Energy b L=0.5mH Single Pulse		25	mJ	
TJ	Operation junction temperature		-55~150	$^{\circ}$	
T _{STG}	Storage temperature range		-55~150		

➤ Thermal Resistance Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance a	36	°C ///	
$R_{ heta JC}$	Junction-to-Case Thermal Resistance	10	°C/W	

Note:

- a. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with T_A=25 °C. The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.

SSC-V1.1 www.sscsemi.com Analog Future



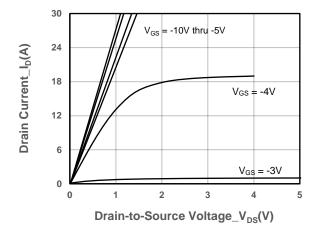


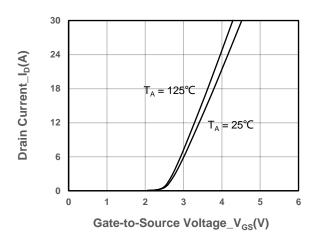
> Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-40			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250uA$	-1	-1.5	-2.5	V
Drain-Source On-Resistance	R _{DS(on)}	$V_{GS} = -10V, I_D = -7A$		22	32	mΩ
		V _G S = -4.5V, I _D = -4A		30	40	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -40V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	lgss	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			±100	nA
Forward Voltage	V_{SD}	V _{GS} = 0V, I _S = -7A		-0.85	-1.3	V
Gate Resistance	R _G	$V_{DS} = 0V, f = 1MHz$		11		Ω
Input Capacitance	C _{ISS}	V 20V V 0V		1320		pF
Output Capacitance	Coss	$V_{DS} = -20V$, $V_{GS} = 0V$, $f = 1MHz$		130		
Reverse Transfer Capacitance	C _{RSS}	I = IIVIIIZ		118		
Total Gate Charge	Q_{G}	V 40V V 20V		16		nC
Gate to Source Charge	Q _{GS}	$V_{GS} = -10V, V_{DS} = -20V,$ $I_{D} = -10A$		4		
Gate to Drain Charge	Q _{GD}	ID = -10A		65		
Turn-on Delay Time	T _{D(ON)}			11		
Rise Time	Tr	V _{GS} = -10V, V _{DS} = -10V,		11		
Turn-off Delay Time	$T_{D(OFF)}$	$R_L = 10\Omega, R_G = 1\Omega$		22		ns
Fall Time	Tf			8		
Diode Recovery Time	Trr	I _F =-20A, di/dt=500A/us		18		ns
Diode Recovery Charge	Qrr	I _F =-20A, di/dt=500A/us		16		nC



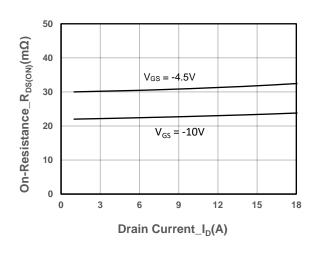
\triangleright Typical Performance Characteristics (T_A=25°C unless otherwise noted)

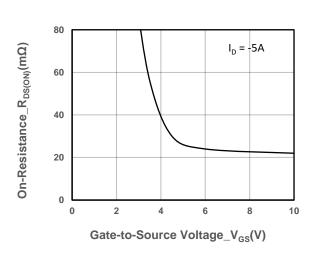




Output Characteristics

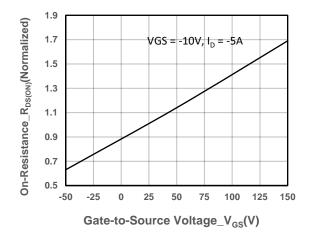
Transfer Characteristics

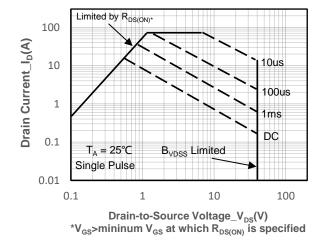




On-Resistance vs. Drain Current and Gate Voltag

On-Resistance vs. Gate-to-Source Voltage



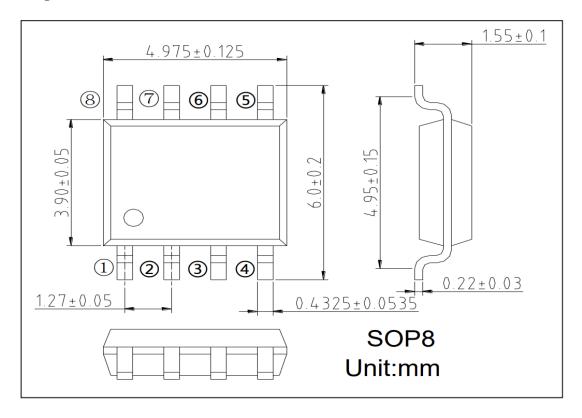


On-Resistance vs. Junction Temperature

Safe Operating Area vs. Junction-to-Ambient



Package Information



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