



SSC8021GS8

P-Channel Enhancement Mode MOSFET with ESD Protection

➤ Features

VDS	VGS	RDS(on) Typ.	ID	ESD
-20V	±12V	0.6R@-4V5	-1A	2kV
		0.8R@-2V5		

➤ Description

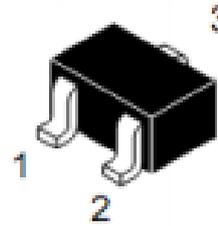
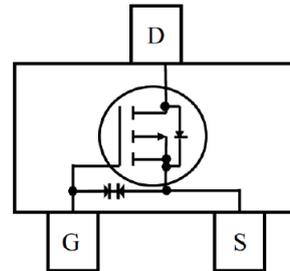
This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package. The product does not contain Rohs substances such as lead and halogen.

➤ Applications

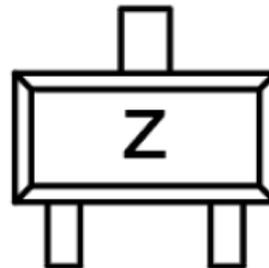
- Load Switch
- Portable Devices
- DCDC conversion

➤ Pin configuration

Top view



SOT-523



Marking

➤ Ordering Information

Device	Package	Shipping
SSC8021GS8	SOT-523	3000/Reel



➤ **Absolute Maximum Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current ^a	-1	A
I_{DM}	Pulsed Drain Current ^b	-2.7	A
P_D	Power Dissipation ^c	0.36	W
P_{DSM}	Power Dissipation ^a	0.22	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance		568	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		347	

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with $T_A=25^{\circ}\text{C}$.The value in any given application depends on the user is specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

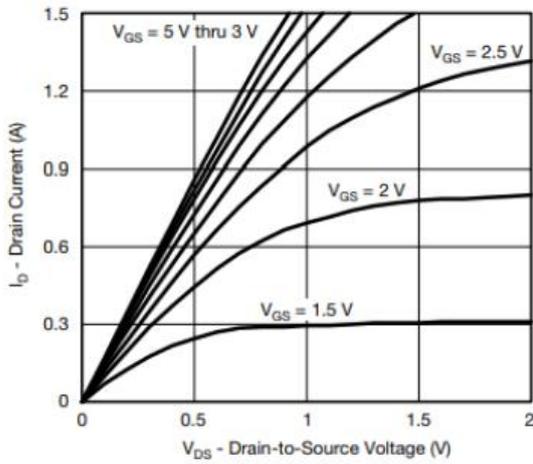


➤ **Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

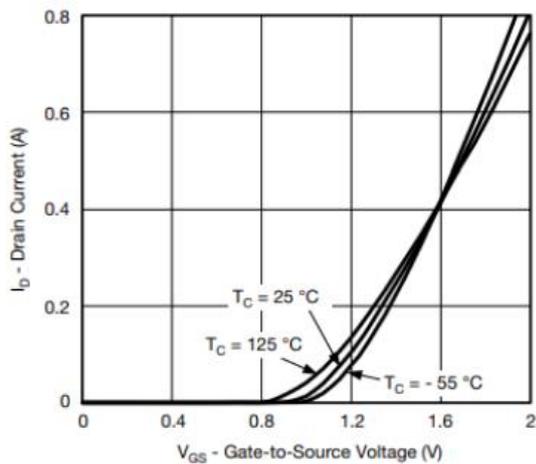
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-0.7	-1	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=-4.5V, I_D=-0.5A$		600	750	mR
		$V_{GS}=-2.5V, I_D=-0.5A$		800	1000	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-16V, V_{GS}=0V$			-1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			± 10	μA
G_{FS}	Transconductance	$V_{DS}=-5V, I_D=-0.45A$		1.5		S
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=-0.15A$			-1.2	V
C_{iss}	Input Capacitance	$V_{DS}=10V, V_{GS}=0V,$ $F=200KHZ$		105		pF
C_{oss}	Output Capacitance			22		
C_{rss}	Reverse Transfer Capacitance			18		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=6V,$ $V_{GEN}=4.5V, R_L=6R,$ $R_G=6R, I_D=0.5A$		54		ns
T_r	Rise time			85		
$T_{D(OFF)}$	Turn-off delay time			890		
T_f	Fall time			176		



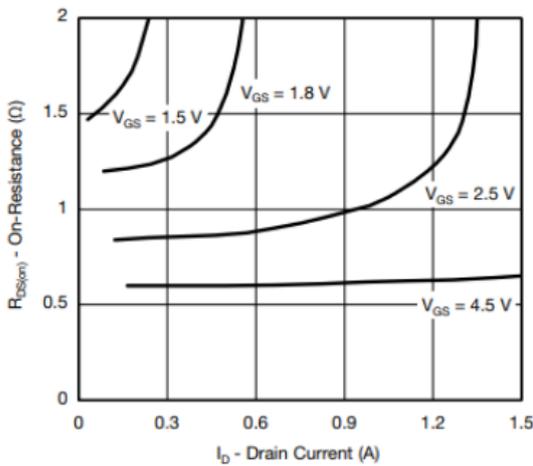
➤ **Typical Characteristics** ($T_A=25^\circ\text{C}$ unless otherwise noted)



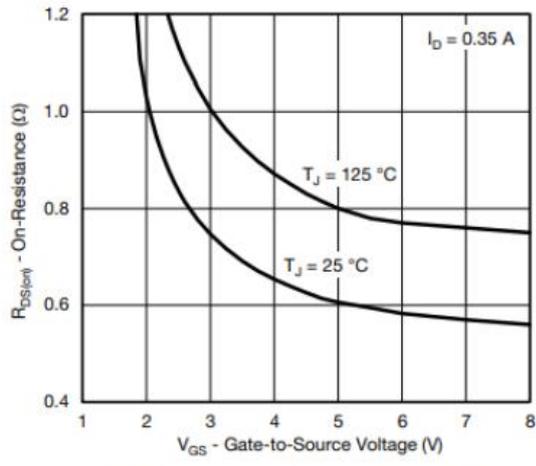
Output Characteristics



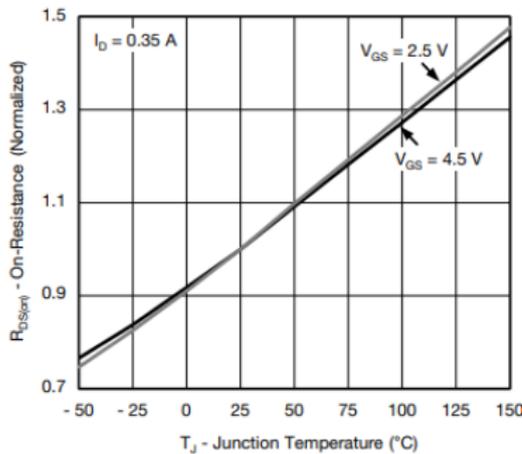
Transfer Characteristics



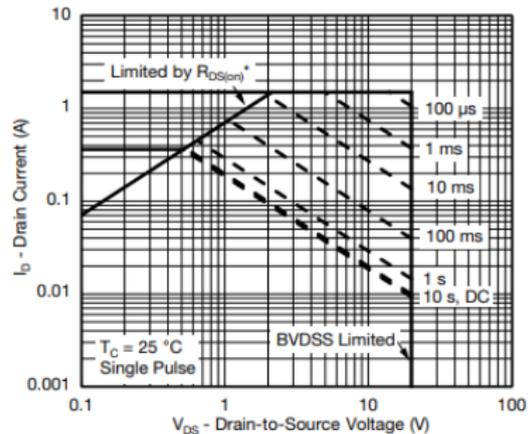
On-Resistance vs. Drain Current



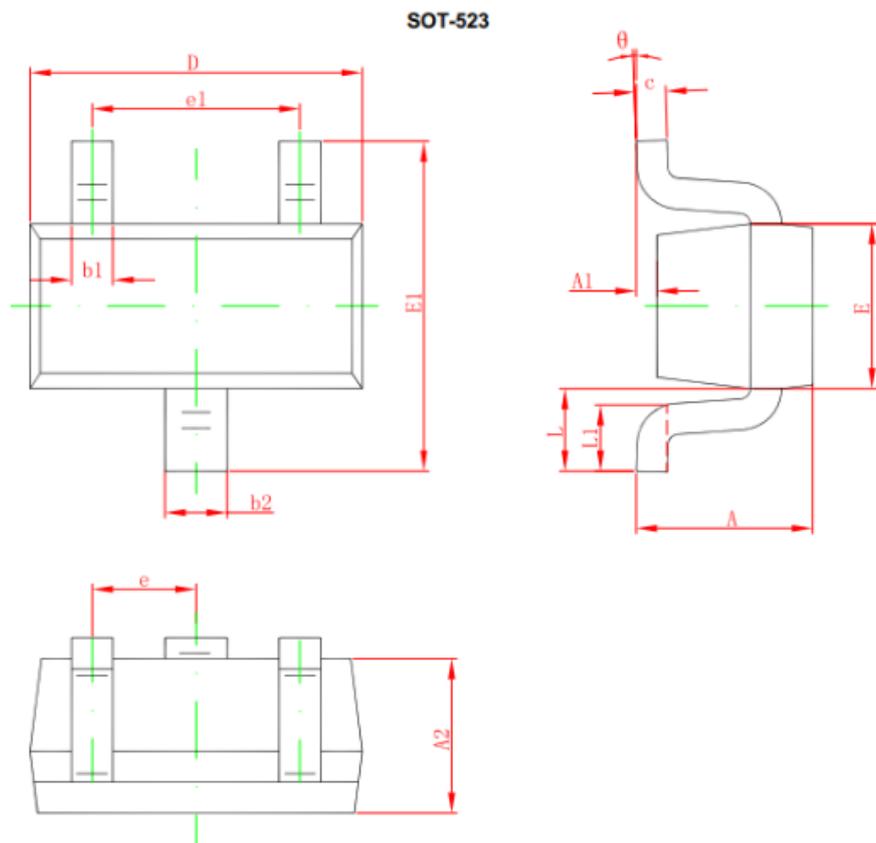
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature



Safe Operating Area, Junction-to-Ambient

➤ Package Information


Symbol	Dimension in Millimeters	
	Min.	Max.
A	0.700	0.900
A1	0.000	0.100
A2	0.700	0.800
b1	0.150	0.250
b2	0.250	0.350
c	0.100	0.200
D	1.500	1.700
E	0.700	0.900
E1	1.450	1.750
e	0.500 Typ.	
e1	0.900	1.100
L	0.400 Ref.	
L1	0.260	0.460
θ	0°	8°



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