

SSC8035GSB

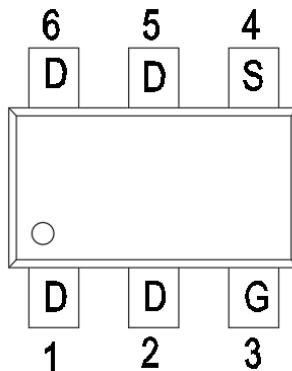
P-Channel Enhanced MOSFET

➤ Features

VDS	VGS	RDS(on) Typ.	ID
-30V	±12V	44mR@-10V	-4.5A
		52mR@-4V5	
		68mR@-2V5	

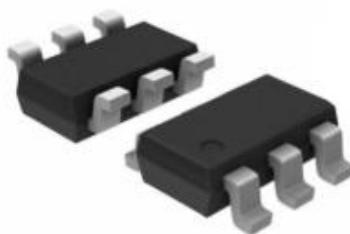
➤ Pin configuration

Top view



➤ Description

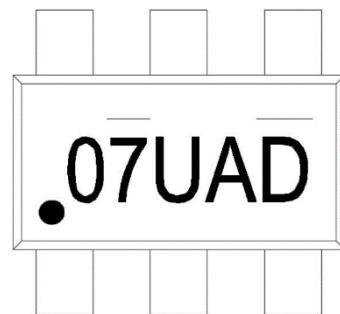
The SSC8035GSB is P-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent RDS(on) with low gate charge. This device is suitable for use in DC-DC conversion and power switch applications.



➤ Applications

- Load Switch
- Portable Switch
- DCDC conversion
- Charging
- Driver for Relay, Motor, Solenoid, LED etc.

SOT-23-6L



Marking

➤ Ordering Information

Device	Package	Shipping
SSC8035GSB	SOT-23-6L	3000/Reel

➤ **Absolute Maximum Ratings($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-30	V
V_{GSS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current ^a	-4.5	A
I_{DM}	Pulsed Drain Current ^b	-22	A
P_D	Power Dissipation ^c	1.6	W
P_{DSM}	Power Dissipation ^a	0.98	W
T_J	Operation junction temperature	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^\circ\text{C}$

➤ **Thermal Resistance Ratings($T_A=25^\circ\text{C}$ unless otherwise noted)**

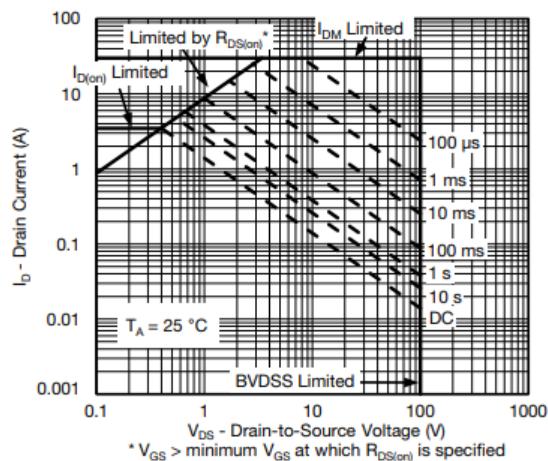
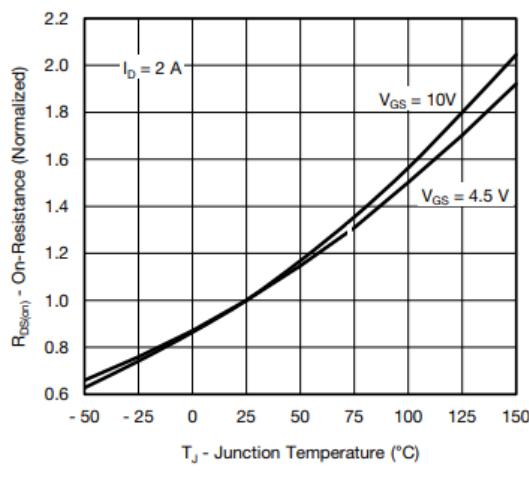
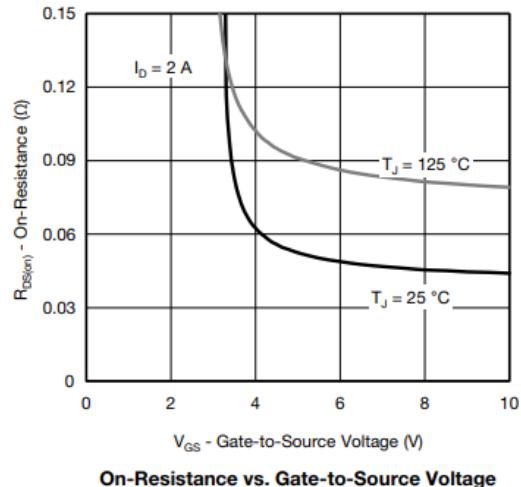
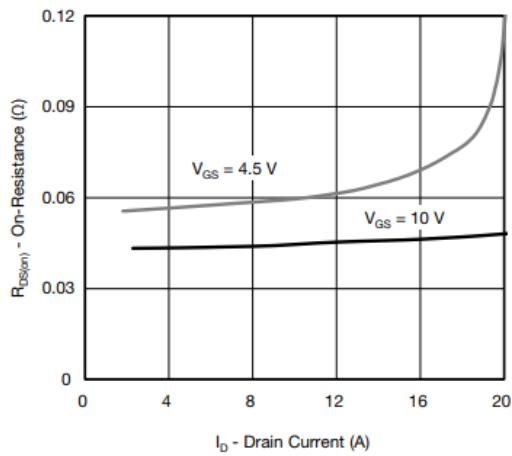
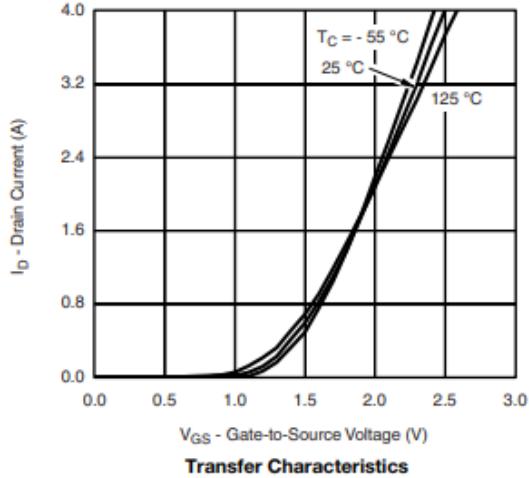
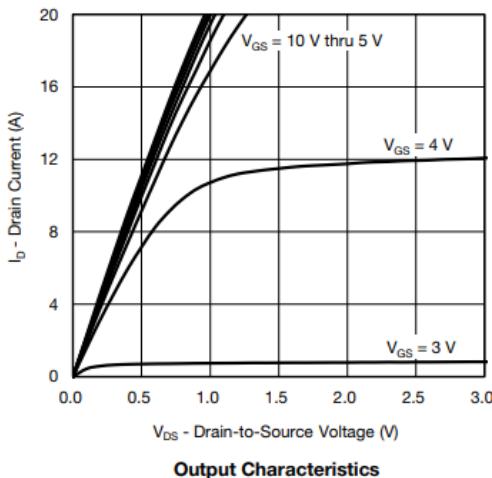
Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		129	$^\circ\text{C/W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		80	

Note:

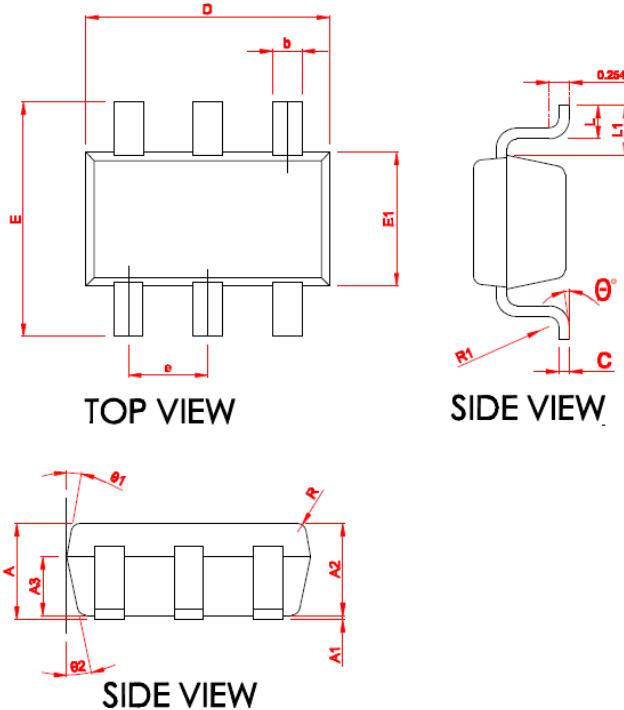
- a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with $T_A=25^\circ\text{C}$.The value in any given application depends on the user specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➤ Electronics Characteristics($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $ID=-250\mu A$	-30			V
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $ID=-250\mu A$	-0.6	-0.9	-1.2	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-10V$, $ID=-4A$		44	65	mR
		$V_{GS}=-4.5V$, $ID=-2A$		52	75	
		$V_{GS}=-2.5V$, $ID=-1A$		68	100	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30V$, $V_{GS}=0V$			-1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 12V$, $V_{DS}=0V$			± 100	nA
G_{FS}	Transconductance	$V_{DS}=-10V$, $ID=-5A$		9		s
V_{SD}	Forward Voltage	$V_{GS}=0V$, $IS=-2A$			1.3	V
C_{iss}	Input Capacitance	$V_{DS}=-15V$, $V_{GS}=0V$, $f=1MHz$		1001		pF
C_{oss}	Output Capacitance			121		
C_{rss}	Reverse Transfer Capacitance			100		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=-10V$, $RL=15R$ $V_{DS}=-15V$, $RG=6R$, $ID=-4.2A$		11		ns
Tr	Rise time			6		
$T_{D(OFF)}$	Turn-off delay time			49		
Tf	Fall time			11		
Q_G	Total Gate Charge	$V_{GS}=-10V$, $V_{DS}=-15V$ $ID=-4.2A$		16		nC
Q_{GS}	Gate to Source Charge			2.3		
Q_{GD}	Gate to Drain Charge			3.1		

➤ **Typical Characteristics($T_A=25^\circ\text{C}$ unless otherwise noted)**


➤ Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.15	1.24
* A1	0.01	0.05	0.09
* A2	1.05	1.10	1.15
A3	0.65	0.70	0.75
* b	0.30	0.35	0.45
* c	0.117	0.127	0.157
* D	2.87	2.92	2.97
* E	2.72	2.80	2.88
* E1	1.55	1.60	1.65
* e	0.90	0.95	1.00
* L	0.32	0.40	0.48
* L1	0.55	0.60	0.65
R	0.10 REF		
R1	0.12 REF		
* θ	0	--	8°
θ1	8°	10°	12°
θ2	10°	12°	14°

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