



## SSC8169GS6

### P-Channel Enhancement Mode MOSFET

#### ➤ Features

$V_{DS}$	$V_{GS}$	$R_{DS(ON)}$ Typ.	$I_D$
-60V	$\pm 20V$	155m $\Omega$ @-10V	-2.1A
		185m $\Omega$ @-4V5	

#### ➤ Description

The This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

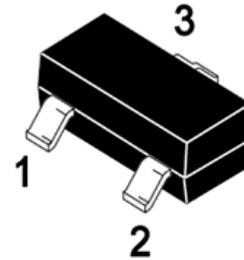
#### ➤ Applications

- Load Switch
- Portable Devices
- DCDC Conversion

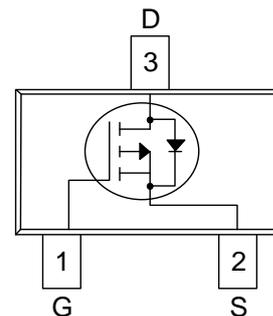
#### ➤ Ordering Information

Device	Package	Shipping
SSC8169GS6	SOT-23	3000/Reel

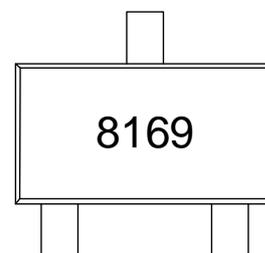
#### ➤ Pin configuration



**SOT-23**



**Pin Configuration (Top View)**



**Marking**



➤ **Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	-60	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>a</sup>	-2.1	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	-8	A
$P_D$	Power Dissipation <sup>a</sup>	1.14	W
$T_J$	Operation junction temperature	-55~150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55~150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>	110	$^{\circ}\text{C}/\text{W}$

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with  $T_A=25^{\circ}\text{C}$ . The value in any given application depends on the user is specific board design. The power dissipation is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.

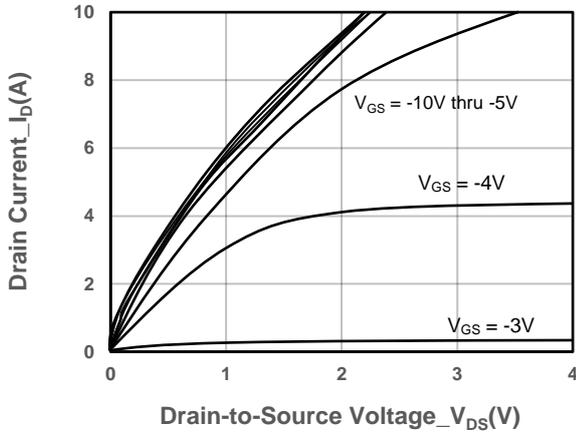


➤ **Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

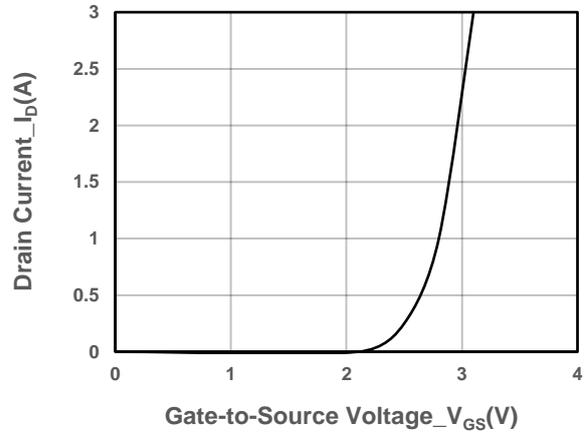
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250uA	-1	-2	-3	V
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A		155	215	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -1A		185	260	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60V, V <sub>GS</sub> = 0V			-1	μA
Gate-Source Leak Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V			±100	nA
Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1.2A		-0.8	-1.3	V
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V, f = 1MHz		510		pF
Output Capacitance	C <sub>OSS</sub>			31		
Reverse Transfer Capacitance	C <sub>RSS</sub>			21		
Turn-on Delay Time	T <sub>D(ON)</sub>	V <sub>DS</sub> = -30V, I <sub>D</sub> = -1.2A, R <sub>L</sub> = 6Ω, V <sub>GS</sub> = -10V, R <sub>G</sub> = 3Ω		7.2		ns
Rise Time	T <sub>r</sub>			21		
Turn-off Delay Time	T <sub>D(OFF)</sub>			37		
Fall Time	T <sub>f</sub>			12		
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> = -30V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -1.2A		12		nC
Gate to Source Charge	Q <sub>GS</sub>			2.1		
Gate to Drain Charge	Q <sub>GD</sub>			2.4		



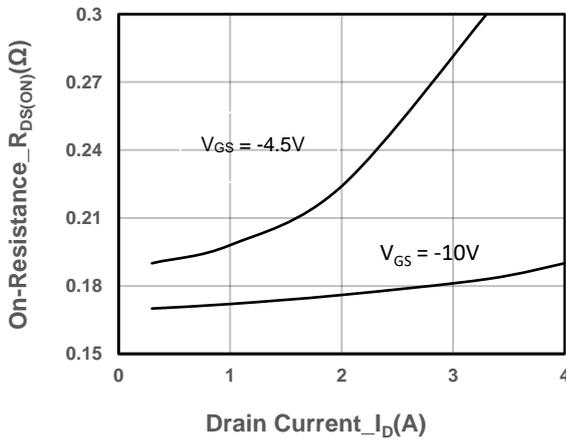
➤ Typical Performance Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise noted)



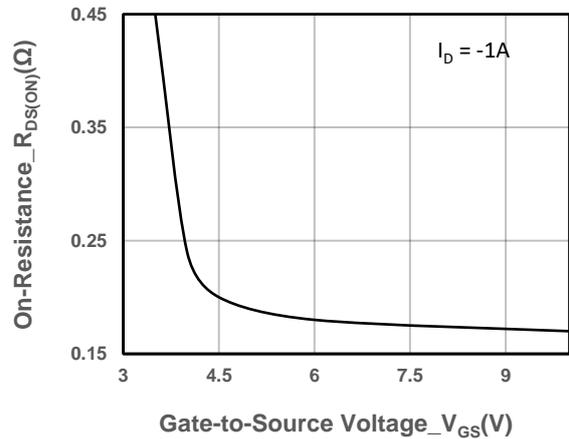
**Output Characteristics**



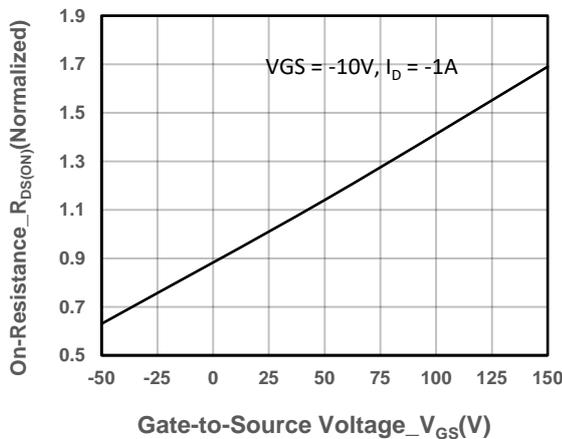
**Transfer Characteristics**



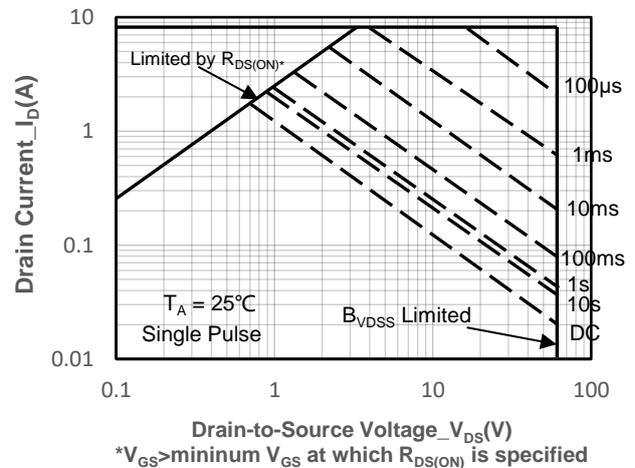
**On-Resistance vs. Drain Current and Gate Volt**



**On-Resistance vs. Gate-to-Source Voltage**

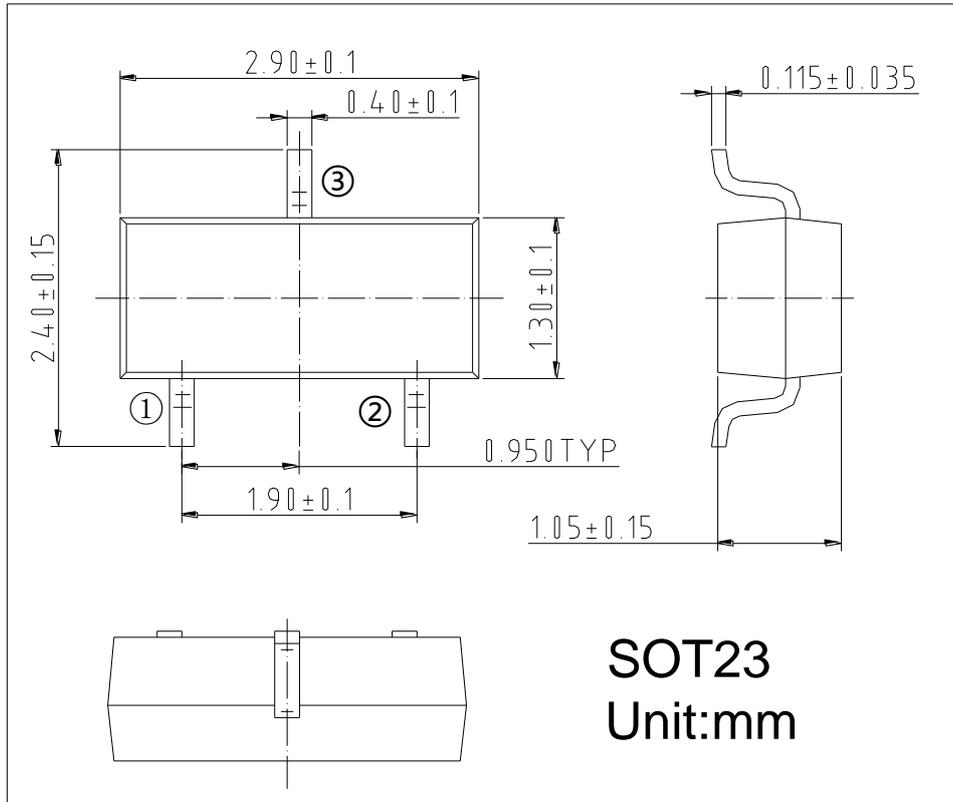


**On-Resistance vs. Junction Temperature**

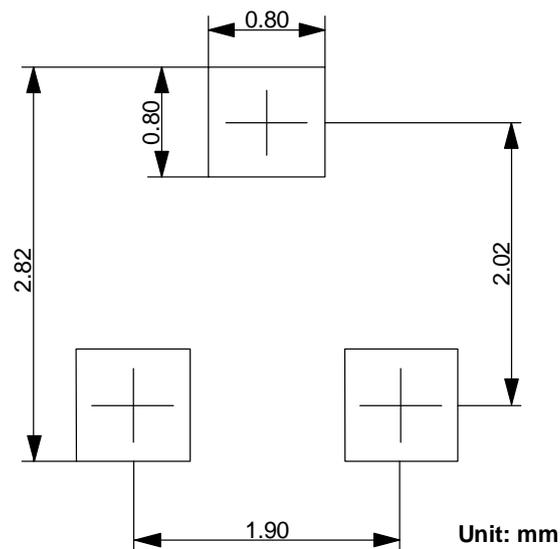


**Safe Operating Area vs. Junction-to-Ambient**

## ➤ Package Information



## ➤ Suggested Pad Layout





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