SSC8P30AN2

N-Channel Enhancement Mode MOSFET with PNP Transistor

➢ Features

N-Channel

VDS	VGS	RDSON Typ.	ID
30V	±10V	330mR@4V5	1A
		440mR@2V5	
		700mR@1V8	

PNP Transistor

VCE	VBE	VCESAT Typ.	IC
-40V	-6V	-160mV	-1A

➢ Description

SSC8P30AN2 combines an N-Channel enhancement mode power MOSFET which is produced with high cell density and a Media Power PNP Transistor. The tiny and thin outline saves PCB consumption.

➢ Applications

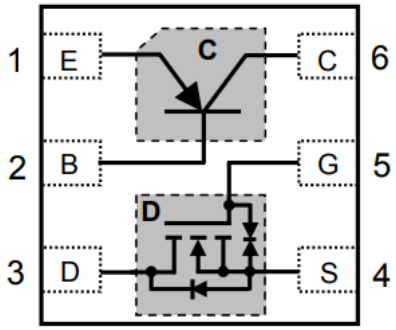
- Li-Battery Charging
- Other power management in portable equipments

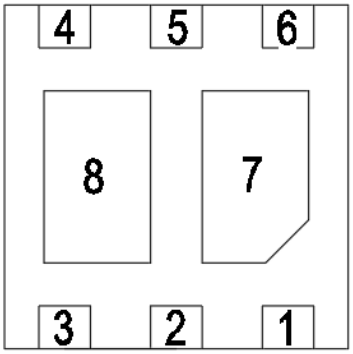
➢ Ordering Information

Device	Package	Shipping
SSC8P30AN2	DFN2X2	3000/Reel

➢ Pin configuration

Top view





Bottom View

Marking

➢ **Absolute Maximum Ratings**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
N-MOS			
V_{DSS}	Drain-to-Source Voltage	30	V
V_{GSS}	Gate-to-Source Voltage	±10	V
I_D	Continuous Drain Current [a]	1	A
I_{DM}	Pulsed Drain Current [b]	3	A
PNP Transistor			
V_{CBO}	Collector-Base Voltage	-40	V
V_{CEO}	Collector-Emitter Voltage	-40	V
V_{EBO}	Emitter-Base Voltage	-6	V
I_C	Collector Current [a]	-1	A
I_{CM}	Pulsed Collector Current [b]	-2	A
Power Dissipation and Temperature			
P_D	Power Dissipation [c]	3.3	W
P_{DSM}	Power Dissipation [a]	1.25	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ **Thermal Resistance Ratings**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		100	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		38	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

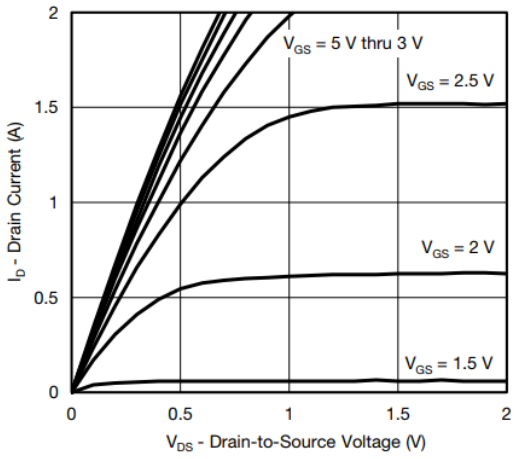
c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

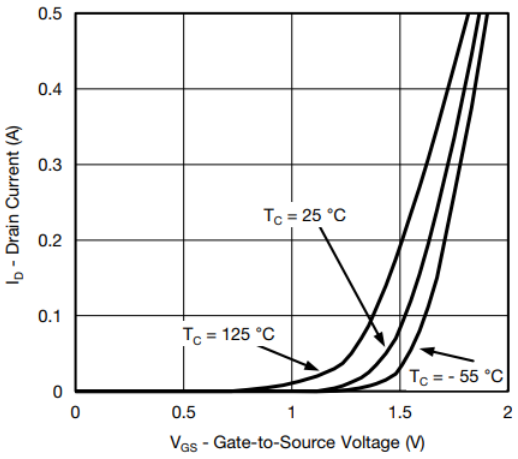
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
N-Channel Enhancement Mode MOSFET						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V , ID=250uA	30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS , ID=250uA	0.5	0.85	1.2	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=4.5V , ID=0.5A		330	450	mR
		VGS=2.5V , ID=0.5A		440	650	
		VGS=1.8V , ID=0.3A		700	1200	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=24V , VGS=0V			1	uA
I_{GSS}	Gate-Source leak current	VGS=±10V , VDS=0V			±10	uA
V_{SD}	Forward Voltage	VGS=0V , IS=1A		0.7	1.3	V
G_{FS}	Transconductance	VDS=5V , ID=0.5A		2.4		S
Ciss	Input Capacitance	VDS=24V , VGS=0V, f=100KHz		80		pF
Coss	Output Capacitance			40		
Crss	Reverse Transfer Capacitance			10		
$T_{D(ON)}$	Turn-on delay time	VDS=10V, VGS=4.5V, RL=10R, RG=6R , ID=0.3A		43		ns
Tr	Turn-on Rise time			92		
$T_{D(OFF)}$	Turn-off Delay time			710		
Tf	Turn-off Rise time			430		

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
PNP Transistor						
BVCBO	Collector-Base Breakdown Voltage	IC=-100uA IE=0	-40			V
BVCEO	Collector-Emitter Breakdown Voltage	IC=-1mA IB=0	-40			V
BVEBO	Emitter-Base Breakdown Voltage	IE=-100uA IC=0	-6			V
ICBO	Collector cut off current	VCB=-35V IE=0			-0.1	uA
IEBO	Emitter cut off current	VEB=-4V IC=0			-0.1	uA
HFE	DC Current Gain	VCE=-1V IC=-0.1A	100		360	
VCESAT	Collector-Emitter Saturation Voltage	IC=-0.8A IB=-80mA		-0.16	-0.5	V
VBESAT	Base-Emitter Saturation Voltage	IC=-0.8A IB=-80mA		-0.9	-1.2	V
f_T	Transition frequency	VCE=-6V, IE=-0.02A f=30MHz	150			MHz

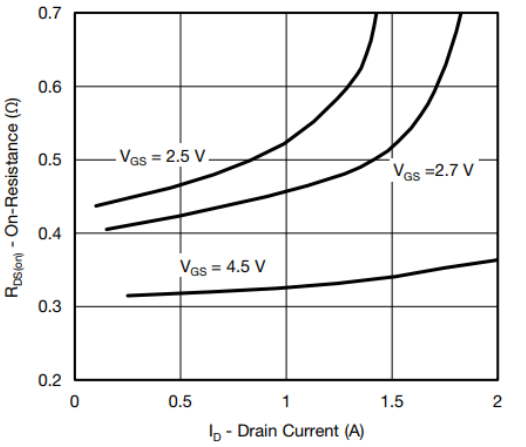
➢ N-Channel Typical Characteristics(T_A=25℃ unless otherwise noted)



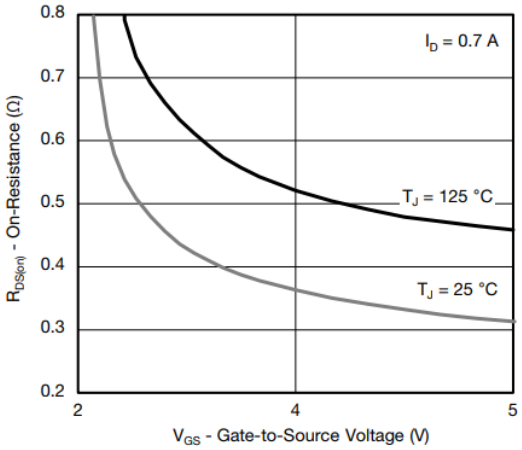
Output Characteristics



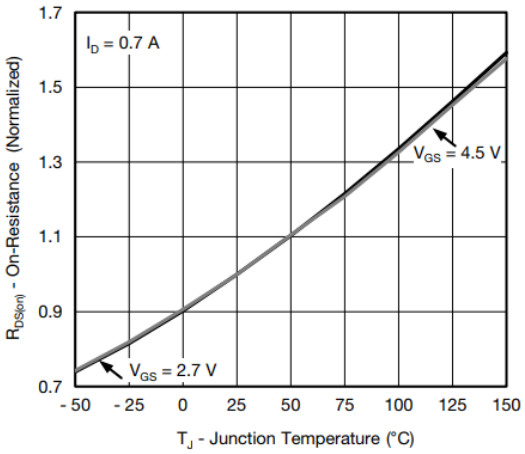
Transfer Characteristics



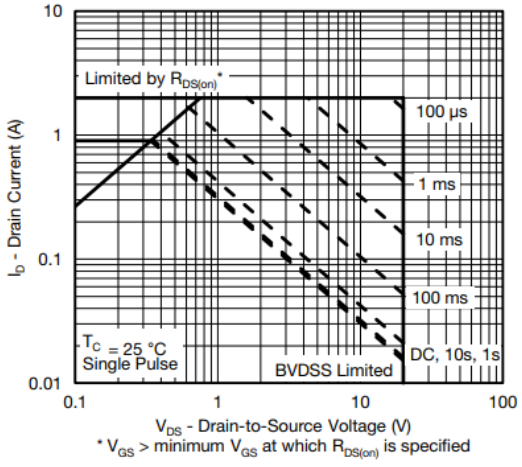
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage

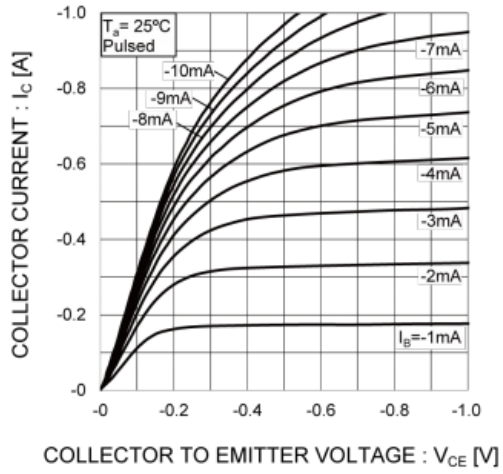


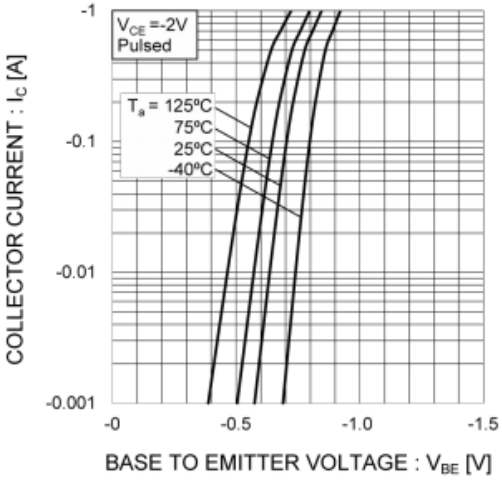
On-Resistance vs. Junction Temperature

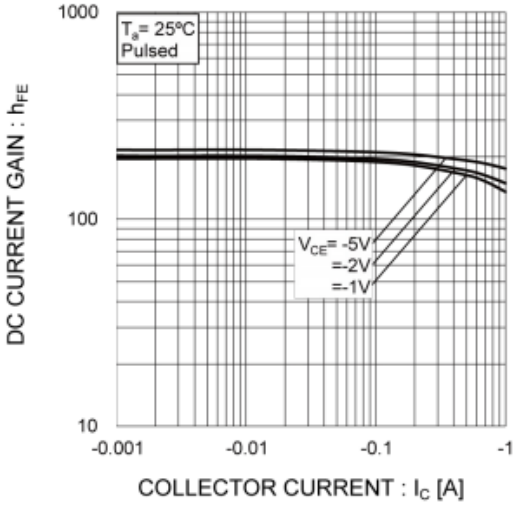


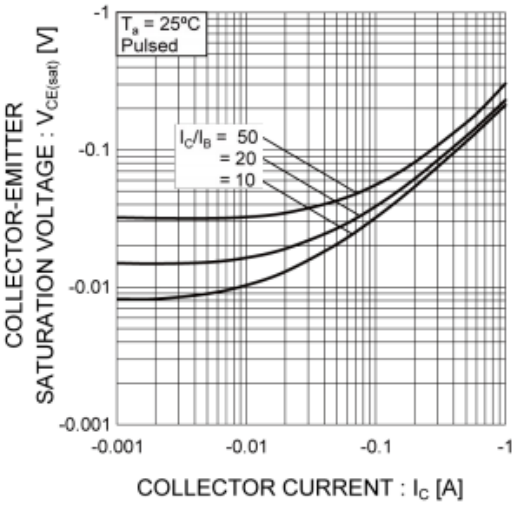
Safe Operating Area, Junction-to-Ambient

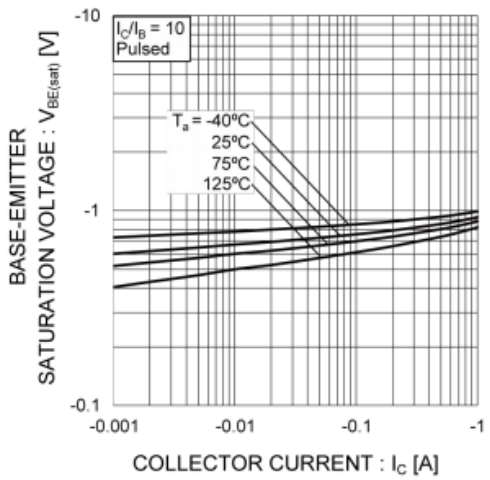
➢ PNP Transistor Typical Performance Characteristics

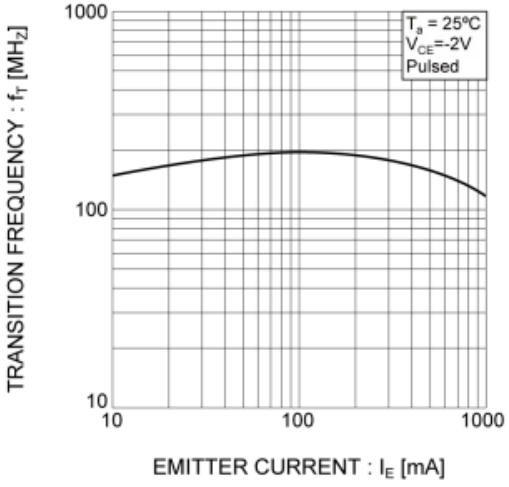




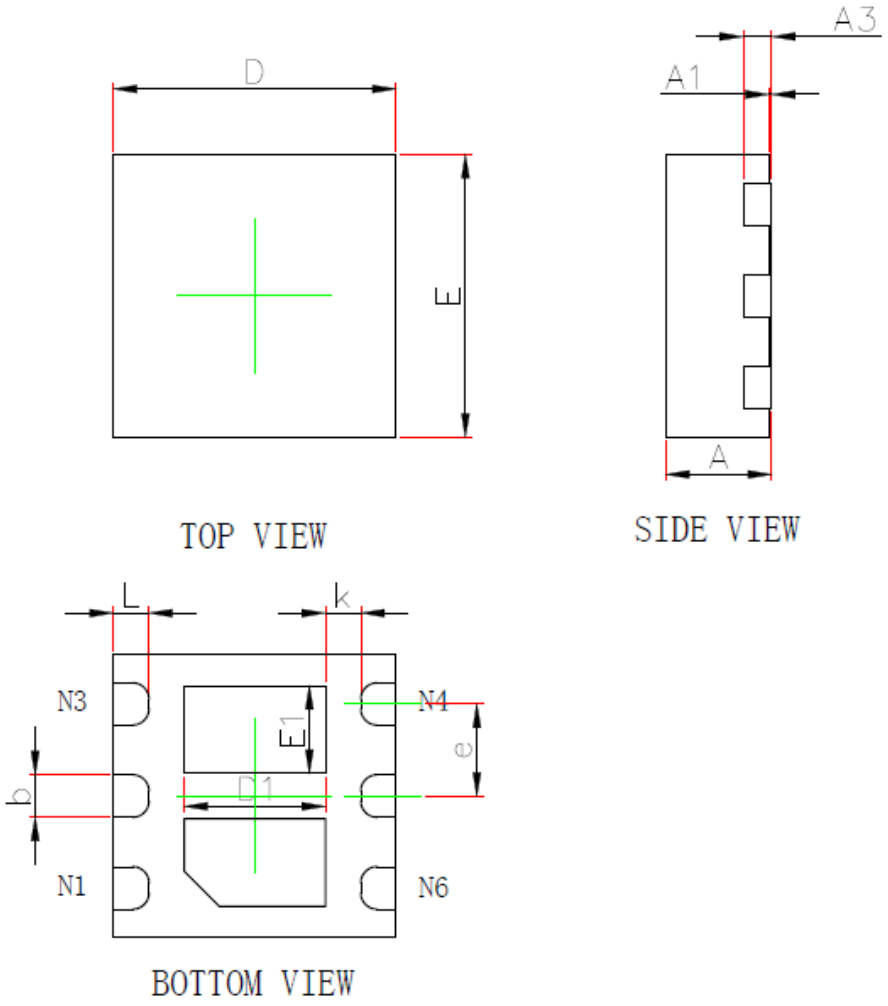








➢ Package Information



DFN2X2-8L

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E1	0.520	0.720	0.020	0.028
b	0.250	0.350	0.010	0.014
e	0.650TYP.		0.026TYP.	
k	0.200MIN.		0.008MIN.	
L	0.200	0.300	0.008	0.012

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